ISIE 2011 Tutorial Proposal

Switched-Capacitor DC-DC Converters:
From Understanding Basics to Systematic Algebraic and Topological Approach

Scheduled Lecturer
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Objectives and audience
The objective of this tutorial is three-fold. We will start with historical notes and some SC basics. In the first part we will briefly review known modeling approaches and from this perspective we will refer to and discuss an elegant and computationally efficient mathematical modeling tool formely integrated into the SC literature by the author. The introduced notion of Incremental Graph will serve throughout this tutorial as the basis for understanding how converter works and as the theoretical foundation and methodology for advanced derivations in modeling and analysis. A variety of applications will be on display.
The second part will be devoted to selected synthesis issues. A topological approach presented has a power of resolving many of the intriguing problems in power electronics circuit systematization. The modeling tool above will be dedicated both to lossless SC DC-DC topological synthesis and to efficient loss calculations. The third part will deliver numerous design examples, comments and links to commercially available converters and charge pumps.
A tutorial is of intermediate level addressed mainly to attendees like low and medium power switched capacitor DC-DC systems’ designers, researchers in the fields of circuits and systems, selected postgraduate and PhD students. The scheduled stuff from nature is to be more aimed at academic circles. However, a tutorial material and style is planned to be both theoretically rigorous and practically relevant. In so doing and with numerous illustrative design examples planned, techniques including hand calculations and Pspice simulations, a presentation will be easily accesible for practitioners. Consequently the author believes that such a tutorial may be sought after by the ISIE target audience.

Synopsis
Switched capacitor (SC) DC-DC converters or just charge pumps remain in modern power electronics vein. The circuits historically originated in AC-DC capacitor-diode voltage multipliers and may be represented by the Cockcroft-Walton invention. Modern DC-DC history started in 1976 [2] with Dickson charge pump in integrated technology. A research on SC DC-DC converters still however, remains in developing stage. The results in the literature are scattered around numerous case studies [3], differ by modeling approaches [1], [4], [9] and yield ambiguous conclusions open to a number of alternative explanations [5], [7].
In our tutorial we will refer to and discuss an elegant and computationally efficient mathematical modeling tool formely introduced into a literature by the author. The notion of Incremental Graph we speak about arose from application of graph theory and linear algebra, takes a unified topological combined-matrix form. The model emerging has some ‘magic’ in it and is capable to cover and handle such various converter specifications as attainable voltage gain, equivalent output/input resistance and its optimization, performance degradation due to parasitic stray capacitances, different working modes and power efficiency in two-phase converters. The modeling procedure starts with a proper re-arrangement of KVL balance equations to a Fibonacci-Hessenberg matrix form. Loss calculations call for incremental cut-set matrices of the same incremental form. Systematic switching circuit solutions are given for even and odd converters respectively. The second part will be devoted to selected synthesis issues. For instance a switched-capacitor converter has a theoretical potential of realizing any fractional and integer voltage ratio (gain) within limits established [9] however details on systematic constructing a circuit with specific programmed gain are a mystery.
A topological approach presented has a power of resolving this and some/most of the intriguing problems in switched circuits systematization [12], problems still unsolved or addressed like: minimum component count and minimal canonical structures, generating of all attainable discrete voltage gains targeted to fine voltage regulation, loss reduction and improved power efficiency (much attention has been paid in academia and industry to this problem [4-14]). We will mainly concentrate on converters working in the so called slow switching limit. Some model extensions are to be signalized with applications to: discrete component converter versus integrated charge pump with loss and output resistance minimization, power efficiency optimization (the latter two are not the same), multi-phase gains, converters working in fast switching limit and resonant switched-capacitor-based converters [11]. Just to have a sample of the presentation and results achieved we show a result on minimum component count SC voltage regulator synthesized.

### Detailed synthesis of two-phase minimum component count SC voltage regulators: attainable sets of voltage gains

Let’s start with a simple circuit consisting of \( k = 4 \) capacitors and say it initially realizes integer voltage gains only. Still however, a designer is faced with a certain variety of alternative and competitive approaches and circuit solutions. In our procedure we begin with Fibonacci Ternary Number System to get a set of realizable integer gains \( M \) (in bold).

<table>
<thead>
<tr>
<th>( \pi )</th>
<th>0</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>( M )</td>
<td>([0]_F = 0)</td>
<td>([1]_F = 2)</td>
<td>([2]_F = 4)</td>
</tr>
<tr>
<td>( \pi )</td>
<td>([0]_F = 1)</td>
<td>([1]_F = 3)</td>
<td>([2]_F = 5)</td>
</tr>
<tr>
<td>( \pi )</td>
<td>([0]_F = 2)</td>
<td>([1]_F = 4)</td>
<td>Number of representations = 8</td>
</tr>
</tbody>
</table>

Example : \( k = 4 \) capacitors, \( M_{\text{max}} = 5 \). The number of representations in our Fibonacci Base System is given by \( F_{k+1} \)

To construct a CP the sums make the entries: \( [0]_F = [0] - [0] \) or \([1] - [1]\); \( [1]_F = [1] - [0] \); \( [2]_F = [1] - [-1] \)

A number of switches required \( \pi \) remains in the predicted limit \( \pi_{\pi} \leq 3k - 2 = 10 \) [8], [9].

<table>
<thead>
<tr>
<th>( \pi )</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \pi )</td>
<td>10</td>
<td>8</td>
<td>7</td>
<td>5 (4)</td>
</tr>
</tbody>
</table>

Rules of thumb, circuit diagrams in switching phases and complete diagrams with implemented switches will follow.

The third part will deliver a set of instructive and handy examples and designs to feel a taste of the approach and prove a reasonable compromise between math involved, circuit model complexity and practical relevance. Links to commercially available converters and charge pumps will be given.

### Selected references and materials

Outline and provisional schedule | Tutorial length
---|---
3 hours (half day)

INTRODUCTION
- Historical roots and origin of switched-capacitor converters
- Switched-Capacitor versus (inductive) PWM DC-DC converters
- Pros and cons of switched-capacitor converters

PART 1 (50 min)
1. **Topological formulation and solution of the switched-capacitor network problem**
   1.1 Historical review
   1.2 Kirchhoff Laws and topological matrices. Solvability of the system of combined linear equations
   1.3 Systematic Modeling of Switched Capacitor DC-DC Converters with Incremental Graph Approach
   1.4 Lossless model – a pure topological solution
   1.5 Minimum component count and minimal canonical structures
   1.6 Complete set of realizable voltage gains
   1.7 Lossy model – dependencies on circuit parameters and parasitics
   1.8 Equivalent circuits
   1.9 Model extensions and applications

PART 2 (55 min)
2. **Switched capacitor converter synthesis**
   2.1 Translating incremental matrices into topologies (even/odd, integer/fractional gain converters)
      2.1.1 Fibonacci Ternary Number System
      2.1.2 Fibonacci-Hessenberg Matrices partition into realizable topological matrices
      2.1.3 Complete diagrams and switch inclusion
   2.2. Selected synthesis issues
      2.2.1. Discrete voltage regulation and fine tuning
      2.2.2. Voltage regulation block with power efficiency optimization
      2.2.3. Discrete component converters versus integrated charge pumps
      2.2.4. Performance limits of multi-phase converters
      2.2.5. Switched-Capacitor-Based converters
   2.3. Comparison to existing topologies and synthesis approaches
   2.4. Open problems

PART 3 (45 min)
3. **Theory versus practical relevance – engineering notes**
   3.1. Review of existing and commercially available solutions
   3.2. Can they be improved ?
   3.3. Discussion on possible modifications and improvements
   3.4. Design examples, hand calculations and design procedures
   3.5. Computer (Pspice and Matlab) simulations
   3.6. Comments and conclusions

• Q&A